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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/591,863	09/06/2006	Simon Deleonibus	129344	3443

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EXAMINER	
KUO, WENSING W	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/591,863	DELEONIBUS, SIMON	
	Examiner	Art Unit	
	W. Wendy Kuo	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 3-5 are pending.

2. The cancellation of claims 1 and 2, and the addition of claims 3-5 in the reply filed on 14 February 2008 obviates the rejection of claim 1 under 35 U.S.C. 112, second paragraph, and the rejection is withdrawn.

3. The copy of the English language translation of the certified priority document (French Application No. 0403066 filed on 25 March 2004) submitted with the reply filed on 14 March 2008 is acknowledged.

Claim Objections

4. Claim 4 is objected to because of the following informalities: an "and" should be deleted (claim 4, line 7). Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claim 4 is rejected under 35 U.S.C. 102(e) as being anticipated by Tezuka et al. (US 7,009,200) (hereinafter Tezuka).

Tezuka (e.g. Figures 1A-1C) teaches a normally on PMOS field effect transistor comprising:

- A source 34 formed by a source material,
- A drain 35 formed by a drain material, and

- A channel formed by a channel material,
- The source, the drain, and the channel materials being selected such that (refer to Figure 1C):
    - An upper level of a valence band of the drain material is higher than an upper level of a valence band of the channel material, and
    - An upper level of a valence band of the source material is lower than the upper level of the valence band of the channel material

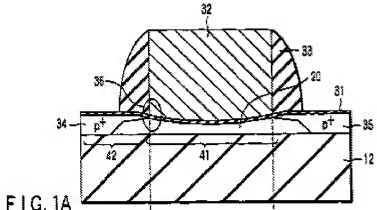

FIG. 1A

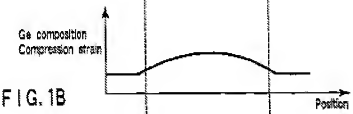

FIG. 1B

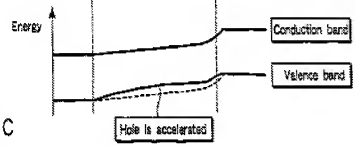

FIG. 1C

Claim Rejections - 35 USC § 103

7. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

8. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tezuka in view of Furukawa et al. (US 4,885,614) (hereinafter Furukawa) and Hall (US 2,918,396) (hereinafter Hall).

9. With respect to claim 3, Tezuka (e.g. Figures 4A-4C) teaches a normally on NMOS field effect transistor comprising:

- A source 34 formed by a source material,
- A drain 35 formed by a drain material, and
- A channel 52 formed by a channel material,
- The source, the drain, and the channel materials being selected such that:
- An electronic affinity of the drain material (SiGe) is lower than an electronic affinity of the channel material (Si) (column 4, lines 59-60)

Tezuka further teaches the use of a $Si_{1-u-v}Ge_uC_v$ ($1>u\geq 0$, $1>v\geq 0$) layer for the source material (column 8, lines 24-27).

*Note that it is inherent that the electronic affinity of germanium is less than the electronic affinity of silicon, and that the electronic affinity of silicon is less than the electronic affinity of the diamond allotrope of carbon.

Tezuka fails to explicitly teach that an electronic affinity of the source material is higher than the electronic affinity of the channel material because Tezuka does not disclose which allotrope of carbon is used in the $Si_{1-u-v}Ge_uC_v$ layer, and Tezuka does not explicitly teach the benefits of using a silicon-carbon alloy (without germanium).

Furukawa teaches that the diamond structure of carbon is used in a silicon-germanium-carbon alloy in order to decrease the misfit dislocation in alloyed

semiconductor devices (column 1, lines 40-42) because the diamond structure of carbon contributes a smaller lattice constant to the alloy (column 3, lines 16-23).

Hall teaches that silicon carbide is a desirable material to use in the fabrication of semiconductor transistors because it can remain extrinsic at high temperatures, whereas devices fabricated using germanium do not function effectively at elevated temperatures because of a reduced contribution from minority carrier injection processes at a P-N junction (column 1, lines 32-51).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the transistor of Tezuka having a $Si_{1-u-v}Ge_uC_v$ source material with the diamond structure of carbon of Furukawa for the benefit of decreasing the misfit dislocation in alloyed semiconductor devices because the diamond structure of carbon contributes a smaller lattice constant to the alloy and to further provide the transistor of Tezuka as modified by Furukawa with the silicon-carbon alloy of Hall for the benefit of fabricating a semiconductor transistor that can remain extrinsic at high temperatures.

10. With respect to claim 5, Tezuka teaches an integrated circuit (column 1, lines 39-41), comprising:

- Normally on PMOS type and normally on NMOS type field effect transistors (column 7, lines 55-58), wherein:
- The normally on NMOS field effect transistor comprises (refer to Figures 4A-4C):
- An NMOS source 34 formed by an NMOS source material,
- An NMOS drain 35 formed by an NMOS drain material, and

- An NMOS channel 52 formed by an NMOS channel material,
- The NMOS source, NMOS drain, and NMOS channel materials being selected such that:
- An electronic affinity of the drain material (SiGe) is lower than an electronic affinity of the channel material (Si) (column 4, lines 59-60)

Tezuka further teaches the use of a $Si_{1-u-v}Ge_uC_v$ ($1>u\geq 0$, $1>v\geq 0$) layer for the source material (column 8, lines 24-27).

*Note that it is inherent that the electronic affinity of germanium is less than the electronic affinity of silicon, and that the electronic affinity of silicon is less than the electronic affinity of the diamond allotrope of carbon.

- The normally on PMOS field effect transistor comprising (refer to Figures 1A-1C):
- A PMOS source 34 formed by a PMOS source material,
- A PMOS drain 35 formed by a PMOS drain material, and
- A PMOS channel formed by a PMOS channel material,
- The PMOS source, the PMOS drain, and the PMOS channel materials being selected such that (refer to Figure 1C):
    - An upper level of a valence band of the PMOS drain material is higher than an upper level of a valence band of the PMOS channel material, and
    - An upper level of a valence band of the PMOS source material is lower than the upper level of the valence band of the PMOS channel material

Tezuka fails to explicitly teach that an electronic affinity of the NMOS source material is higher than the electronic affinity of the NMOS channel material because

Tezuka does not disclose which allotrope of carbon is used in the $Si_{1-u-v}Ge_uC_v$ layer, and Tezuka does not explicitly teach the benefits of using a silicon-carbon alloy (without germanium).

Furukawa teaches that the diamond structure of carbon is used in a silicon-germanium-carbon alloy in order to decrease the misfit dislocation in alloyed semiconductor devices (column 1, lines 40-42) because the diamond structure of carbon contributes a smaller lattice constant to the alloy (column 3, lines 16-23).

Hall teaches that silicon carbide is a desirable material to use in the fabrication of semiconductor transistors because it can remain extrinsic at high temperatures, whereas devices fabricated using germanium do not function effectively at elevated temperatures because of a reduced contribution from minority carrier injection processes at a P-N junction (column 1, lines 32-51).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the NMOS transistor of Tezuka having a $Si_{1-u-v}Ge_uC_v$ source material with the diamond structure of carbon of Furukawa for the benefit of decreasing the misfit dislocation in alloyed semiconductor devices because the diamond structure of carbon contributes a smaller lattice constant to the alloy and to further provide the transistor of Tezuka as modified by Furukawa with the silicon-carbon alloy of Hall for the benefit of fabricating a semiconductor transistor that can remain extrinsic at high temperatures.

Response to Arguments

11. Applicant's arguments with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. Wendy Kuo whose telephone number is (571)270-1859. The examiner can normally be reached Monday through Friday 7:00 AM to 4:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached at (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leonardo Andújar/
Primary Examiner, Art Unit 2826

W. Wendy Kuo
Examiner
Art Unit 2826

WWK